Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SHIGERU ATSUMI

Appeal No. 2003-2078
Application No. 09/028,276

HEARD: Feb. 19, 2004

Before BARRY, LEVY, and BLANKENSHIP, *Administrative Patent Judges.*
BARRY, *Administrative Patent Judge.*

DECISION ON APPEAL

A patent examiner rejected claims 1-9, 13, 14, and 21-42. The appellant appeals therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The invention at issue on appeal concerns an integrated circuit ("IC") integrating a plurality of transistors in one chip. According to the appellant, most conventional ICs feature transistors having gate oxide films of the same thickness. (Spec. at 1.) His specification, (*id.* at 3), however, describes problems that result from the use of such a structure in memories "that utilize a wide range of voltages." (Appeal Br. at 4.)

Accordingly, the appellant forms transistors having different thicknesses of gate oxide film on the same semiconductor substrate. More specifically, transistors having a thicker film are connected directly to external terminals (e.g., input/output terminals, power supply terminals), and transistors having a thinner film are not directly connected to the external terminals. (*Id.* at 3.)

A further understanding of the invention can be achieved by reading the following claim.

1. A semiconductor integrated circuit device comprising:

> a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and
>
> an input/output terminal formed on the semiconductor substrate, wherein a transistor physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Claims 1, 2, and 21-26 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,471,373 ("Shimizu"). Claims 3-9, 13, 14, and 27-42 stand rejected under 35 U.S.C. § 103(a) as obvious over Shimizu.

OPINION

Rather than reiterate the positions of the examiner or the appellant *in toto*, we address the main point of contention therebetween. The examiner asserts, "Shimizu

(Figs. 1-3, 18) discloses . . . an input/output terminal (5) formed on the substrate, wherein a transistor (QE2) physically connected directly to the input/output terminal, absent any intervening elements, being one of the transistors other than a transistor having the thinnest gate insulation film." (Examiner's Answer at 3.) He explains, "[u]pon close inspection of the passage (column 6, lines 66-68), one will see that what the appellant interprets as an aluminum wire connecting the input/output pad with the gate of the transistor, is actually the patterned gate itself." (*Id.* at 5.) The appellant argues, "assuming that the aluminum (interconnection layer 31) is the patterned gate itself per the Examiner's Answer, that does not provide a teaching or suggestion that the transistor QE2 is physically connected directly to input/output terminal 5. . . ." (Reply Br. at 3.)

In addressing the point of contention, the Board conducts a two-step analysis. First, we construe claims at issue to determine their scope. Second, we determine whether the construed claims are anticipated or would have been obvious.

1. CLAIM CONSTRUCTION

"Analysis begins with a key legal question -- *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Here, independent claim 1 recites in pertinent part the following limitations:

"an input/output terminal formed on the semiconductor substrate, wherein a transistor physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film." Similarly, independent claim 21 recites in pertinent part the following limitations: "an input/output terminal formed on the semiconductor substrate, wherein a transistor connected directly to the input/output terminal, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film." Also similarly, independent claim 32 recites in pertinent part the following limitations: "an input/output terminal formed on the semiconductor substrate, wherein a transistor always connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film." Giving the independent claims their broadest, reasonable construction, the limitations require that a transistor having a thicker gate insulation film that other transistors in the same IC be connected directly to an input/output terminal of the IC.

2. ANTICIPATION AND OBVIOUSNESS DETERMINATIONS

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "A claim is anticipated only if each and every element as set forth in the claim is found, either

expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)). "[T]here is no anticipation 'unless all of the same elements are found in exactly the same situation and united in the same way . . . in a single prior art reference.'" *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894, 221 USPQ 669, 673 (Fed. Cir. 1984) (citing *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983).

Here, Shimizu discloses "an improved EPROM (Electrically Programmable Read Only Memory) device, and a method of manufacturing the same." Col. 1, ll. 8-11. The EPROM device includes "a semiconductor substrate 1 (semiconductor pellet) which . . . has arranged on part of its major surface a memory array portion 2 constructed of a plurality of MIS type memory transistors each of which has a gate electrode of a two-layered structure." Col. 2, ll. 23-28. "Terminals for external connections 5 are arrayed along the marginal edge parts of the substrate 1." *Id.* at ll. 35-37. Figure 18 of the reference, a "process sectional view[] of [a] step[] in one method of manufacturing [the] EPROM device," *id.* at ll. 7-8, shows "an enhancement

type MIS transistor Q_{E2} for writing . . . as [an] MIS type transistor[]. . . ." Col. 7, ll. 7-10. The Figure also shows "Al (aluminum) . . . evaporated onto the substrate 10 and . . . patterned to thereby form an interconnection layer 31." Col. 6, l. 66 - col. 7, l. 1. We are not persuaded, however, that the interconnection layer 31 connects the transistor Q_{E2} to any of the terminals for external connections 5.

"In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "'A *prima facie* case of obviousness is established when the teachings from the prior art itself would . . . have suggested the claimed subject matter to a person of ordinary skill in the art.'" *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

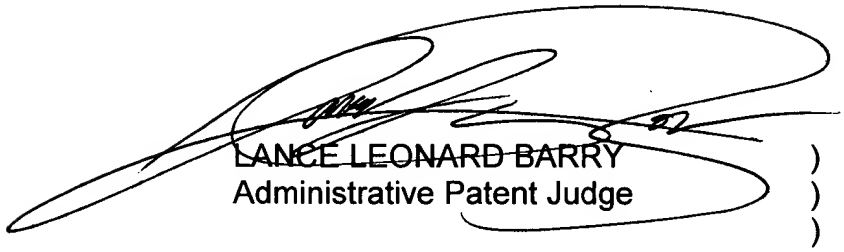
Here, absent a teaching or suggestion of that the transistor Q_{E2} is connected to any of the terminals for external connections 5 via the interconnection layer 31 let alone directly connected thereto, we are unpersuaded of a *prima facie* case of obviousness. Therefore, we reverse the rejections of claim 1; of claims 2-9, 13, and 14; of claim 21; of claims 22-31; of claim 32; and of claims 33-42, which depend therefrom.

CONCLUSION

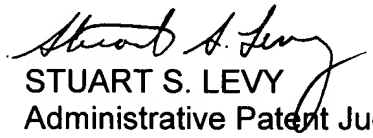
In summary, the rejection of claims 1, 2, and 21-26 under § 102(b) is reversed.

The rejection of claims 3-9, 13, 14, and 27-42 under § 103(a) is also reversed.

REVERSED



LANCE LEONARD BARRY
Administrative Patent Judge



STUART S. LEVY
Administrative Patent Judge

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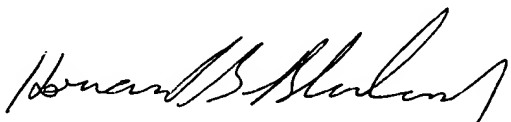

HOWARD B. BLANKENSHIP
Administrative Patent Judge

BANNER & WITCOFF LTD.
11TH FLOOR
1001 G STREET NW
WASHINGTON, DC 200014597